Abstract of the Disclosure:

An integrated magnetoresistive semiconductor memory in which each memory cell contains a switching transistor or a diode in the form of an activatable isolating element, and two magnetic layers that are isolated by a thin tunnel barrier. Connecting conductors are respectively integrated for word lines, digit lines and bit lines and also for the purpose of activating the switching transistor in one or more memory cells. These connecting conductors are located in only two metallization planes and in a polysilicon connection plane.

MPW/kf